MICROPROCESSOR BASED SYSTEMS

CMP 410

LECTURE 2

My site
https://AssemSite8.wix.com/site8
**ORG**

Directive used by assembler to define the start address of the next machine code at the program memory

Such as **ORG 0**, **ORG 100h**
END

• Directive used by assembler.
• Any instruction after it consider as comment.

```
MOV A, #FFH
```

Program M
The machine cycle (MC) is the minimum number of CPUs (12 CPUs) taken by CPU to perform a single instruction cycle (F-D-E).
The internal clock pulse

Uses by CPU to synchronize all process of the microcontrollers

$$f_{\text{crystal}}/12$$

$$F = f_{\text{crystal}}$$
The rate of machine cycles
(internal clock pulses)

Crystal Oscillator
(Up to 24 MHz) → Internal clock divider by 12 → Rate of the Internal clock pulses

Rate of Machine cycle = \(\frac{\text{Crystal frequency}}{12}\) [MHz]
Calculate the rate of the internal clock pulse of AT89C55 if the external crystal with frequency 3 MHz

The answer

\[
\text{The Rate of internal clock pulse} = \frac{\text{Crystal frequency}}{12} = \frac{3 \times 10^6}{12} = 250 \text{ KHz}
\]
The Execution time

Is time taken by CPU to carry out an instruction

The Run-time (Delay-time)

Is time taken by CPU to carry out program or subprogram
EXAMPLE

Calculate the total run-time (total delay time) for AT89C51 during execution of 3 instructions that need 1, 2 and 4 machine cycles respectively, the connected crystal has frequency equal 6 MHz.

The answer

\[
\text{Delay time} = \frac{\text{Total number of Machine cycles} \times 12}{\text{Crystal frequency}}
\]

\[
= \frac{(4 + 2 + 1) \times 12}{6} = 14 \text{ \mu sec}
\]
The FET as electronic switch
Each terminal of port has

- Flip-Flop
- 2 tri-state buffers
- Output driver (FET)

Quasi bi-directional ports
The ports can output either '1' or '0' at any time.

The ports can accept input '0' at any time but the ports can accept input '1' only if its flip-flop is loaded by '1'.
By Setting the bit (or resetting μC)

- The bit-of-port has output “1”
- It can accept external “1” or “0” after the “READ PIN” is activate
By clearing the bit (or output zero)

- The bit-of-port has output “0”
- It can’t accept any external “1”
The most port’s instructions activate the "READ PIN" to accept the logical inputs from a port to any other register such as (MOV A, P1) or (OR A, P0).
Few port's instructions activate the "READ LATCH" to accept logical inputs from a port to itself such as ORL A.

Before operation

After operation

An operation
The internal memories of 8051
The PC points to the memory location to fetch current instruction.
The Internal Program memory

MOVC A, @A+DPTR

destination  Pointer
Example

MOVC A, @A+DPTR

Val(A+DPTR) = 24h + 0011h = 35h
After executing the instruction `MOVC A, @A+DPTR`

![Diagram showing the execution of the `MOVC A, @A+DPTR` instruction]

- **Address Bus (ext. or int.)**
- **Data Bus (ext. or int.)**

10/8/2018
The internal RAM

- **Special Function Registers (SFR)**: 128 Bytes
- **General Purpose Registers**: 80 Bytes
- **Bit-Addressable Registers**: 16 Bytes
- **Register Bank 0 (Default)**: 8 Bytes
- **Register Bank 1**: 8 Bytes
- **Register Bank 2**: 8 Bytes
- **Register Bank 3**: 8 Bytes

Register Bank:
- R7
- R6
- R5
- R4
- R3
- R2
- R1
- R0
<table>
<thead>
<tr>
<th>Bit Addressable</th>
<th>SFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>F0</td>
<td>F7</td>
</tr>
<tr>
<td>E0</td>
<td>E7</td>
</tr>
<tr>
<td>D0</td>
<td>D7</td>
</tr>
<tr>
<td>B8</td>
<td>-</td>
</tr>
<tr>
<td>B0</td>
<td>B7</td>
</tr>
<tr>
<td>A8</td>
<td>AF</td>
</tr>
<tr>
<td>A0</td>
<td>A7</td>
</tr>
<tr>
<td>99</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>98</td>
<td>9F</td>
</tr>
<tr>
<td>90</td>
<td>97</td>
</tr>
<tr>
<td>8D</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>8C</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>8B</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>8A</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>89</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>88</td>
<td>8F</td>
</tr>
<tr>
<td>87</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>83</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>82</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>81</td>
<td>Not Bit Addressable</td>
</tr>
<tr>
<td>80</td>
<td>87</td>
</tr>
</tbody>
</table>
The Program-Status-Word Register (PSW)

- 4 status flags (CY, AC, P, OV)
- 2 control flags (RS0, RS1)
- User bit addressable flag (F0)
- Reversed flag (bit1)
Selection of operational bank

RS1 | RS0
---|---
1  | 1
1  | 0
0  | 1
0  | 0

Start address

Bank 0
Bank 1
Bank 2
Bank 3

Microprocessor 2017-18
The Carry and Auxiliary carry flags

Carry flag (CY=1)  
such ADD ADDC

Auxiliary Carry flag (AC=1)

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

Accumulator
The parity flag (P)

\[ P = \sum_{\text{bit 0}}^{\text{bit 7}} \text{ones in Accumulator} \]

Odd number \( \rightarrow \) \( P = 1 \)

Even number
Or none ones \( \rightarrow \) \( P = 0 \)
The Over Flow flags (OV = 1) in three cases

- When the divisor has value zero during the division operation.
- When the multiplication product is greater than the value "FFh".
- When an error occurs during the addition and subtraction operations for the *signed numbers* (the result outside the signed 8-bit range "-128" to "127").
Find the status of the flags CY, AC and P after the addition of the two digital values ABh and 38h in AT89C51.

The answer

$$\begin{array}{c|c|c}
\text{Hex} & \text{Binary} \\
\hline
AB & 1010\ 1011 \\
+\ 38 & 0011\ 1000 \\
\hline
\text{E3} & 1110\ 0011 \\
\end{array}$$

**CY = 0** because there isn't carry-up from 8th bit of the final result.

**AC = 1** because there is carry-up from 4th to 5th bit of the final result.

**P = 1** because the Accumulator has odd number of ones (5 ones).
Find the status of the flags CY and OV after the addition of the two digital values F4h and 80h in the AT89C51.

The answer